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| L7 | 1698 | 714/746.ccls. | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2005/10/13 16:38 |
| L8 | 330 | 714/55.ccls. | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2005/10/13 16:38 |
| L9 | 264 | 714/731.ccls. | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2005/10/13 16:39 |
| L10 | 318 | 714/700.ccls. | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2005/10/13 16:40 |
| L11 | 237 | 714/814.ccls. | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2005/10/13 16:40 |
| L12 | 297 | 714/815.ccls. | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2005/10/13 16:41 |
| L13 | 590 | 714/819.ccls. | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2005/10/13 16:42 |
| L14 | 236 | 714/744.ccls. | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2005/10/13 16:43 |
| L15 | 476 | 713/401.ccls. | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2005/10/13 16:44 |

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|-----|-----|---|---|----|-----|------------------|
| L16 | 851 | 713/500.ccls. | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2005/10/13 16:45 |
| L17 | 810 | 713/600.ccls. | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2005/10/13 16:46 |
| L18 | 24 | (circuit\$1 same logic) and (((error\$1 adj control adj code) or ECC) same ((memory or stor\$3) with transparent)) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2005/10/13 17:14 |
| L21 | 0 | (circuit\$1 with transient with disturbance\$1) and (logic with circuit\$1) and ((flipflop\$1 or flip-flop\$1) same (clock\$1 with delay\$3)) and ((analy\$4 or compar\$5) with output\$1 with (flipflop\$1 or flip-flop\$1) with (error\$1 or fault\$1)) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2005/10/13 17:24 |
| L25 | 0 | (combina\$6 adj logic adj circuit\$1) and ((flipflop\$1 or flip-flop\$1) with (clock\$1 with delay\$3)) and ((analy\$4 or compar\$5) with output\$1 with (flipflop\$1 or flip-flop\$1) with (error\$1 or fault\$1)) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2005/10/13 17:29 |
| L27 | 0 | (combina\$6 adj logic adj circuit\$1) and ((flipflop\$1 or flip-flop\$1) with clock) and ((flipflop\$1 or flip-flop\$1) with delay\$3 with output) and ((analy\$4 or compar\$5) with output\$1 with (flipflop\$1 or flip-flop\$1) with (error\$1 or fault\$1)) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2005/10/13 17:34 |
| L29 | 0 | (three adj (identical or "same") adj logic adj circuit\$1) and (preced\$3 with memory with (logic adj circuit\$1)) and (two-input with memory with output\$1 with logic) and (memory with transparent with (identical or "same") with input\$1) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2005/10/13 17:40 |
| L31 | 104 | (combina\$6 adj logic adj circuit\$1) and (flip-flop\$1 with clock\$1 with delay\$3) and (analy\$4 or compar\$5) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2005/10/13 17:45 |

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|-----|----|------------------------|--------------------|----|-----|------------------|
| L37 | 10 | nicolaidis-michael.IN. | US-PGPUB; USPAT | OR | OFF | 2005/10/13 18:07 |
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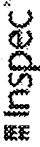
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| #2 ((flip-flop <and> clock <and> delay <and> logic circuit) <in> metadata) | 62 |
| #3 ((identical logic circuits <and> memory <and> transparent) <in> metadata) | 0 |

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